IN THE CLAIMS

1. (Canceled)

2. (Previously Presented) The memory cell of claim 29, wherein materials comprising at least one of the storage electrode and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

3. (Original) The memory cell of claim 2, wherein the barrier energy is selected to obtain a desired data charge retention time of less than or equal to approximately 40 seconds at 250 degrees Celsius.

4. (Original) The memory cell of claim 2, wherein the barrier energy is selected to obtain a desired erase time of less than approximately 1 second.

5. (Original) The memory cell of claim 2, wherein the barrier energy is selected to obtain a desired erase voltage of less than approximately 12 Volts.

6. (Canceled)

7. (Canceled)

8. (Previously Presented) The memory cell of claim 29, wherein the barrier energy is less than approximately 2.0 eV.

9. (Previously Presented) The memory cell of claim 29, wherein the storage electrode is isolated from conductors and semiconductors.

10. (Previously Presented) The memory cell of claim 29, wherein the storage electrode is transconductively capacitively coupled to a channel.

11. (Canceled)

12. (Previously Presented) The memory cell of claim 28, wherein materials comprising at least one of the storage electrode and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

13. (Original) The transistor of claim 12, wherein the barrier energy is selected to obtain a data charge retention time of the transistor that is adapted for dynamic refreshing of charge stored on the floating gate.

14. (Previously Presented) The transistor of claim 28, wherein the floating gate is isolated from conductors and semiconductors.

15-17. (Canceled)

18. (Previously Presented) The transistor of claim 28, wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the barrier energy is less than approximately 2.0 eV; and

an area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

19. (Previously Presented) A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 2.0 eV;

a control electrode, separated from the floating gate by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

20. (Previously Presented) The transistor of claim 28, wherein the floating gate is capacitively separated from the channel region for providing transconductance gain.

21.-27. (Canceled)

28. (Previously Presented) A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate being conductively doped and comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide;

a control electrode, separated from the floating gate by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

29. (Previously Presented) A memory cell comprising:

a storage electrode comprising a material that has a smaller electron affinity than polycrystalline silicon to store charge;

an insulator adjacent to the storage electrode, wherein a barrier energy between the insulator and the storage electrode is less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide;

a control electrode separated from the storage electrode by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

30.-31. (Canceled)

32. (Previously Presented) A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate floating gate being conductively doped and comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV the insulator having a larger electron affinity than silicon dioxide; and

a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

33-34. (Canceled)

35. (Currently Amended) The memory device of claim [[34]] <u>32</u> wherein the barrier energy is selected to obtain a data charge retention time for each transistor that is adapted for dynamic refreshing of charge stored on the floating gate.

36. (Previously Presented) The memory device of claim 32 wherein the floating gate of each transistor is isolated from conductors and semiconductors.

37. (Canceled)

38. (Canceled)

39. (Previously Presented) The memory device of claim 32 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the barrier energy is less than approximately 2.0 eV; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region of each transistor.

40. (Previously Presented) The memory device of claim 32 wherein the floating gate of each transistor is capacitively separated from the channel region for providing transconductance gain.

41. (Previously Presented) The transistor of claim 19 wherein:

an area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

42. (Previously Presented) The memory cell of claim 29, further comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and wherein:

the storage electrode comprises polycrystalline or microcrystalline silicon carbide;

the insulator is between the storage electrode and the channel region, and the barrier energy is less than approximately 2.0 eV; and

an area of a capacitor formed by the control electrode, the storage electrode, and the intergate dielectric is larger than an area of a capacitor formed by the storage electrode, the insulator, and the channel region.

43. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

44. (Previously Presented) The transistor of claim 43 wherein:

the insulator comprises amorphous silicon carbide;

the floating gate comprises polycrystalline or microcrystalline silicon carbide; and

the barrier energy is less than approximately 2.0 eV.

45. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide; and

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

46. (Previously Presented) The transistor of claim 45 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the barrier energy is less than approximately 2.0 eV.

47. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide;

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

48. (Previously Presented) The transistor of claim 47 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide; and

the barrier energy is less than approximately 2.0 eV.

49. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the

channel region.

50. (Previously Presented) The transistor of claim 49 wherein:

the insulator comprises amorphous silicon carbide;

the barrier energy is less than approximately 2.0 eV; and

the floating gate comprises polycrystalline or microcrystalline silicon carbide.

51. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

52. (Previously Presented) The transistor of claim 51 wherein:

the barrier energy is less than approximately 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

53. (Previously Presented) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate

comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 2.0 eV;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

54. (Previously Presented) The transistor of claim 53 wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

the floating gate comprises polycrystalline or microcrystalline silicon carbide.

55. (Previously Presented) A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

56. (Previously Presented) The memory cell of claim 55 wherein:

the insulator comprises amorphous silicon carbide;

the barrier energy is less than approximately 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the

channel region.

57. (Previously Presented) A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

58. (Previously Presented) The memory cell of claim 57 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the barrier energy is less than approximately 2.0 eV; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

59. (Previously Presented) A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate being conductively doped and comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

60. (Previously Presented) The memory cell of claim 59 wherein:

the barrier energy is less than approximately 2.0 eV; and

the floating gate comprises polycrystalline or microcrystalline silicon carbide.

61. (Previously Presented) A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 2.0 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

62. (Previously Presented) The memory cell of claim 61 wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises polycrystalline or microcrystalline silicon carbide; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

63. (Previously Presented) A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

64. (Previously Presented) The memory device of claim 63 wherein:

the insulator comprises amorphous silicon carbide;

the barrier energy is less than approximately 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

65. (Previously Presented) A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier

energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

66. (Previously Presented) The memory device of claim 65 wherein:

the barrier energy is less than approximately 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

67. (Previously Presented) A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 2.0 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

68. (Previously Presented) The memory device of claim 67 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

69. (Previously Presented) A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate being conductively doped and comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

70. (Previously Presented) The memory device of claim 69 wherein:

the barrier energy is less than approximately 2.0 eV;

the floating gate comprises polycrystalline or microcrystalline silicon carbide; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

71. (Previously Presented) The memory device of claim 32, further comprising:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

72. (Canceled)

73. (Previously Presented) A memory cell comprising:

a storage electrode to store charge, the storage electrode being conductively doped and comprising a material that has a smaller electron affinity than polycrystalline silicon;

an insulator adjacent to the storage electrode, wherein a barrier energy between the insulator and the storage electrode is less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide; and

a control electrode, separated from the storage electrode by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

74. (Previously Presented) The memory cell of claim 73, further comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region; and

wherein the insulator is between the storage electrode and the channel region; and

wherein an area of a capacitor formed by the control electrode, the storage electrode, and the intergate dielectric is larger than an area of a capacitor formed by the storage electrode, the insulator, and the channel region.

75. (Previously Presented) A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV, the insulator having a larger electron affinity than silicon dioxide; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

76. (Previously Presented) The memory device of claim 75 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

77. (Previously Presented) A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate being capacitively separated from the channel region to provide transconductance gain, the insulator having a larger electron affinity than silicon dioxide; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

78. (Previously Presented) The memory device of claim 77 wherein:

the floating gate comprises polycrystalline or microcrystalline silicon carbide and has a smaller electron affinity than polycrystalline silicon;

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.